ABSTRACT

The present invention relates to a method for fabricating high performance chip interconnects and packages by providing methods for depositing a conductive material in cavities of a substrate in a more efficient and time saving manner. This is accomplished by selectively removing portions of a seed layer from a top surface of a substrate and then depositing a conductive material in the cavities of the substrate, where portions of the seed layer remains in the cavities. Another method includes forming an oxide layer on the top surface of the substrate such that the conductive material can be deposited in the cavities without the material being formed on the top surface of the substrate. The present invention also discloses methods for forming multi-level interconnects and the corresponding structures.